

**Specification and Simulation of
ALICE DAQ System**

Giovanna Di Marzo Serugendo



Outline

- ❖ Modelling and Simulation Tool
- ❖ ALICE DAQ Specification
- ❖ Current Status and Performances
- ❖ Next Steps



Modelling and Simulation Tool

❖ Foresight (Foresight Systems, Inc.)

- System level modelling and simulation tool
- Performances evaluation

❖ Specification

- Data Flow Diagrams (event-driven processes, events, control flows)
- State Transition Diagrams
- Mini-Specs
- Real-time Parameters



Modelling and Simulation Tool

❖ Analysis

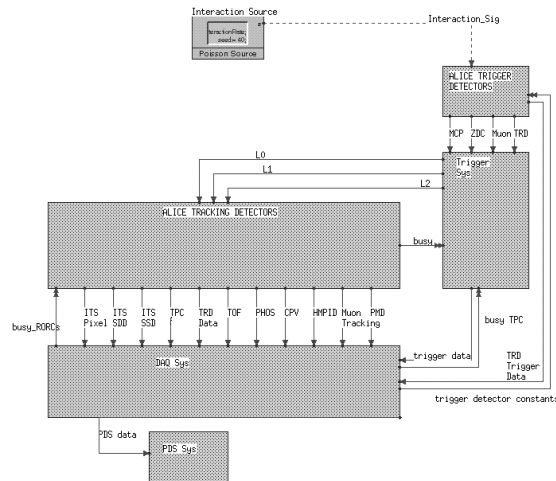
- Type checking, input/output checking, syntax errors

❖ Simulation

- Real-time execution of specification
- Stand-alone executable specification
- Animation of Diagrams
- Real-time constraint validation
- Debugging functions (breakpoints, monitors windows)
- Works on Sun workstation and Windows NT



Specification: Overall Architecture



Trigger System

❖ 3 Levels Trigger

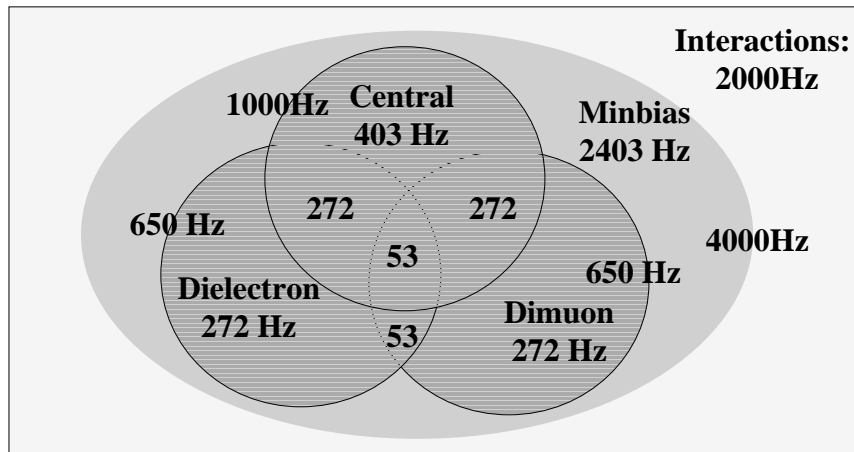
- L0 : performs P/F protection + busy check check at 0, send information at 1.2 μ s.
- L1: performs P/F protection (changes detector classes if necessary) check at 4.3 μ s, send information at 5.5 μ s.
- L2: performs P/F protection (changes detector classes if necessary) check at 88 μ s, send information at 89.2 μ s
- L0, L1, L2 arrives in order (L0 L1 L0' L1' L2 L2' is possible)

❖ Parameters P/F Protection

- dimuon: 3 μ s
- dielectron: 7 μ s
- other: 88 μ s



Event Rates: L0 Input

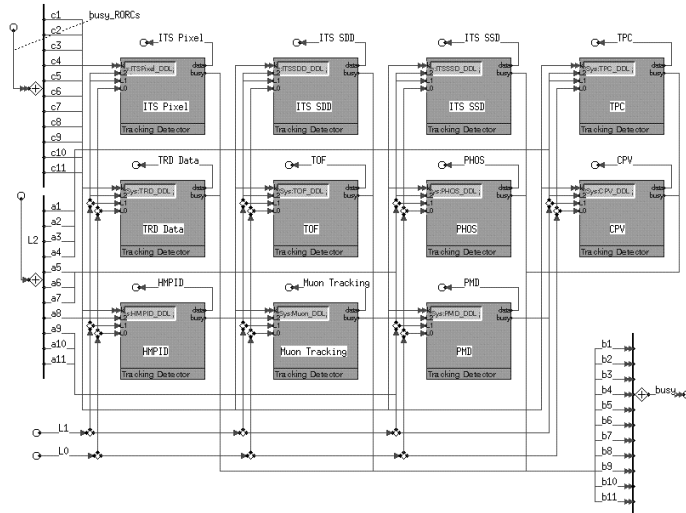


Tracking Detectors

- ❖ Permanently wait for L0 signals
 - If L0 then become immediately “busy”
- ❖ If L0 signal then wait for L1 signal
 - L1 reject => become “not busy”
 - L1 accept => remain busy until end of reading, collects data
- ❖ Multi-buffer for storing data
 - one buffer of 4 positions for each DDL
- ❖ If L1 accept, wait for L2 signal
 - L2 = send, then Data is sent along DDL
 - L2 = throw, data is discarded

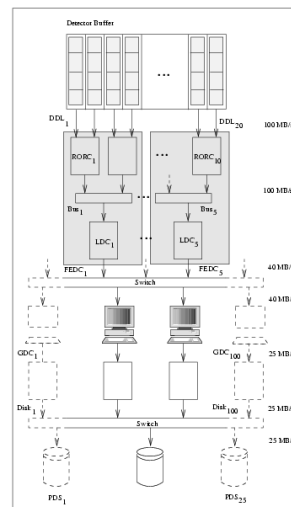


Specification: Tracking Detectors



DAQ Sub-System

- ❖ Detectors Buffer: 4 positions
- ❖ 397 DDLs: 100 Mbytes/s
- ❖ 299 RORCs: Size: 12 Mbytes
- ❖ 240 Bus: 100 Mbytes/s
- ❖ 240 LDCs: Size: 128 Mbytes
 - Sub-event building
- ❖ 100 GDCs: Size: 512Mbytes
 - Event Building
- ❖ 100 Disks: Files of 1 Gbytes
- ❖ 25 PDS: Infinite Buffer



Performances

Infinite Buffer, All Events

	L0	L1	L2	L0 %	L1 %	L2%
Central	248	242	186	3.7	3.6	3
Dimuon	327	324	556	5.2	5.1	9.1
Dielectron	260	252	354	4.3	4.2	5.8
Minbias	1361	1323	798	23	22	13
Misc	385	377		6.5	6.4	
Interaction	1997			33		
Total	6038			100		

After 1 sec (6038 ev)
Poisson (6000 Hz)



Performances

Finite Buffer, Maximal Bandwidth, All Events

	L0	L1	L2	L0 %	L1 %	L2%
Central	79	78	58	1.3	1.3	1
Dimuon	523	517	602	8.7	8.5	9.9
Dielectron	108	104	143	1.8	1.7	2.4
Minbias	535	516	314	8.7	8.5	5.2
Misc	146	142		2.4	2.3	
Interaction	1997			33		
Total	6038			100		

After 1 sec (6038 ev)
Expected at L2:

	C	MB	DM	DIEL	Total
L2	20 Hz	20 Hz	650 Hz	200 Hz	890 Hz



Detectors Parameters**TPC and TRD**

	Bufér Size	Read T.	Reset T.	Transm.	Throw T.	Centr. Up	Centr. Lo
TPC	4	100 μ s	0.1 μ s	18000MB/s	1 μ s	75.9MB	56.1MB
TRD	4	50 μ s	0.1 μ s	1800 MB/s	1 μ s	8 MB	8MB

- Generic Detectors
- TPC, TRD fill buffer
- TRD “worse” than TPC
(has more frequently a full buffer)

**Next Steps**

- ❖ Evaluation of Performances with Real bandwidth
 - Event Rates
 - Verification of Mass Storage capability (1.25 Gbytes/s)
 - Buffer occupancies (for each detector)
- ❖ Architecture Alternatives
 - L2 output
 - GDC choice
- ❖ More Detailed Model
 - DDL detailed specification
 - DAQ Software Framework (DATE) specification

