High-Level System Design Using Foresight

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Outline

- Development Process
- HW/SW Co-Design
- Foresight: a Modelling and Simulation tool
- ALICE DAQ System
Development Process (1)

- Separate Functionality from Architecture
  - Design system functionality before thinking at hardware/software implementation details

- Formal Specification and Verification
  - Mathematical definition of system (unambiguous)
  - Semantics of specification provides a model
  - Behaviour of model = behaviour of system
  - Verification: model behaves correctly (simulation, model checking)

Development Process (2)

- First Phase: Functional Requirements
  - Abstract specification: interfaces, functionality
  - Verification: incomplete/inconsistent functional requirements, performance problems, design errors
  - Analysis: critical parameters, maximum (minimum) performances, particular conditions

- Second Phase: Architectural Concerns
  - Detailed specifications: algorithms, hardware choices, alternative architectures
  - Verification, analysis: check requirements and performances
**HW/SW Co-design**

- Foresight Systems, Inc.
- System Design
  - Foresight tool
  - Specification Execution
- System Co-design
  - Foresight co-design tool
  - Foresight specification with hw/sw components
  - Specification Execution
- HW/SW Components
  - HDL simulation environment
  - Seamless CVE

**Foresight (1)**

- Foresight Tool
  - System Level Modeling and Simulation Tool
- Specification
  - Hierarchical Specifications
  - Data Flow Diagrams (event-driven processes, events, control)
  - State Transitions
  - Mini-specs
  - Real-time parameters
Foresight (2)

- Analysis
  - Type checking, input/output checking, syntax errors

- Execution of Specification (Simulation)
  - Real-time execution of specification
  - Stand-alone executable specification
  - Animation of Diagrams
  - Real-time constraint validation
  - Debugging functions (breakpoints, monitors windows)
  - Simulation is NOT formal verification!
  - Works on Sun workstation

ALICE DAQ

- Model of whole ALICE DAQ System
  - Trigger System (L0, L1, L2)
  - Trigger and Tracking Detectors
  - DAQ (with sub-event building, event building, storage)
  - Parameters (buffer sizes, etc.)

- Evaluation of Performances
  - Whole system: maximal bandwidth / real bandwidth
  - For each detector: buffer occupancy, bandwidth usage

- Alternative Algorithms
  - Event building computing
  - L2 trigger decision
ALICE: Overall System

ALICE: Tracking Detectors
**ALICE: FSM, Mini-Spec**

Results

### Maximal Bandwidth

<table>
<thead>
<tr>
<th></th>
<th>L0</th>
<th>L1</th>
<th>L2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Central</td>
<td>137</td>
<td>133</td>
<td>92</td>
</tr>
<tr>
<td>Dimuon</td>
<td>462</td>
<td>457</td>
<td>585</td>
</tr>
<tr>
<td>Dielectron</td>
<td>159</td>
<td>152</td>
<td>197</td>
</tr>
<tr>
<td>Minbias</td>
<td>747</td>
<td>714</td>
<td>409</td>
</tr>
<tr>
<td>Misc</td>
<td>203</td>
<td>197</td>
<td></td>
</tr>
<tr>
<td>Interaction</td>
<td>1997</td>
<td></td>
<td></td>
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</tbody>
</table>

After 1 sec (6038 ev)

Expected at L2:

<table>
<thead>
<tr>
<th>Buffer Full</th>
<th>Bandwidth</th>
<th>Maximum</th>
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<tbody>
<tr>
<td>TPC</td>
<td>23</td>
<td>14200 MB/18000Mb/</td>
</tr>
<tr>
<td>TRD</td>
<td>43</td>
<td>1627MB/1800MB/</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>C</th>
<th>MB</th>
<th>DM</th>
<th>DIEL</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2</td>
<td>20H</td>
<td>20H</td>
<td>650 Hz</td>
<td>200 Hz</td>
<td>890 Hz</td>
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Conclusion

- Separate Functionality from Architecture
- Foresight Systems provides integrated tools
  - Formal Specification and Execution
  - Seamless replacement of formal components by hardware/software components
  - http://www.nuthena.com/
- Advantage
  - Correct errors before implementation
  - Think about the functional level (correct interfaces)